

# STBook/STylus Expansion Bus Electrical Specification

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## Power Available

External devices must not draw more than 400mA total from VCC on the connector. If the device is to operate on batteries alone, it should not draw more than 100 mA. It is good design practice to use CMOS wherever possible and to shut down power to any circuitry not in use.

## Loading

External devices must not present more than a total of 1 (one) LS-TTL load per line onto the signals. This expansion bus is completely unbuffered, therefore, loading in excess of the recommended amount may cause the system to fail. Open-collector drivers should be prepared to sink 20mA, on those lines which require it, such as /EXPANSION\_WAKE.

## Signal Descriptions

The Atari STBook and STylus can be expanded externally using a 120-pin expansion bus, which is new to these machines. It essentially allows direct access to the 68HC000 address and data buses, and bus control signals to allow appropriate response. There are also the signals to allow for conversion to the previous ROM Cartridge format without the need for active electronics (i.e. a 120-pin expansion to 40-pin ROM cartridge convertor would consist of two connectors and a PCB).

The following signals are all direct from the 68HC000, and need no special description:

o A1-A23	Address Lines
o D0-D15	Data Lines
o /AS	Address Strobe
o /LDS, /UDS	Lower/Upper Data Strobes
o R/W	Read/Write Control
o FC0-FC2	Function Code 0-2
o /VPA	Valid Peripheral Address
o /VMA	
o E	E clock
o /RESET	Reset signal
o /HALT	Halt signal

Two signals are also direct from the 68HC000, but require a bit more operational detail:

o /DTACK	Data Transfer Acknowledge
o /BERR	Bus Error

The Combo chip uses /DTACK to acknowledge memory spaces it controls; it Bus Errors on other spaces (or illegal access to valid spaces) by not generating /DTACK. Other circuitry in the Combo chip times the length of the /AS signal; if it is longer than 16uS, than a /BERR is generated. What this means is that a device on the 120-pin expansion bus can be logically located in address spaces that the Combo chip considers illegal; all that is necessary is to generate a /DTACK early enough such that /AS does not extend to 16uS.

- o /ROM3
- o /ROM4

These two signals are simply the outputs generated by the Combo chip for particular memory spaces, specifically those for the ROM cartridge space. Because the Combo assumes these are ROMs, only reads of this space are acknowledged or selected by the Combo chip. A third signal, /DEV, simply indicates when a peripheral address has been selected in supervisor mode; /DTACK is not necessarily asserted.

- o /DEV
- o /DMA

There is also /DMA, which indicates that a Floppy or ACSI DMA cycle is occurring. It is included because the Combo chip, while asserting /AS and /L/UDS, leaves the address bus in a high-impedance state. Because of the high value pull-up resistors used in the STBook and STylus, the address lines may rise quite slowly when the lines are left in high-impedance. Noise could couple in, and false addresses could be asserted. It is therefore recommended that any address decoding added to the STBook or STylus use /DMA as an additional (active HIGH) qualifier.

- o /BR                      Bus Request
- o /BGACK                Bus Grant Acknowledge
- o /MCUBG                Bus Grant, out from the Combo chip.
- o /CPUBG                Bus Grant, from the CPU to Combo chip  
(this is for reference only)

Use of the Bus Grant system is possible, with some limitations. While the Bus Request and Bus Grant Acknowledge are direct connections to the 68HC000, the Bus Grant signal is an output from the Combo chip. This means that the Combo chip (which includes the Blitter and DMA control) has priority for the gaining control of the Bus; Bus Grant is passed through only if no request is pending internal to the Combo.

- o /EINT3
- o /MFPIEI
- o /MFPIEO
- o /MFPINT
- o /IPL0, /IPL1, /IPL2
- o /IACK

Some interrupt control is also possible, at two separate priority levels. One is a level 3 interrupt, for which an input into the Combo chip priority encoder is provided. For this level, it is the responsibility of the external circuit to respond to the interrupt acknowledge cycle, and to provide a method to clear the interrupt request. Both Auto-Vector and Vectored interrupts are possible.

The external circuitry can also share the Level 6 interrupt with the 68HC901 MFP internal to the STylus and STBook. The external interrupt source can have either higher or (preferably) lower priority than the internal MFP. All of this is accomplished with three signals: /MFPINT, /MFPIEI, /MFPIEO. The first is an open-collector driven, wire-OR signal, indicating a level 6 interrupt. The next two establish the relative priority of the two interrupt sources. /MFPIEI (MFP Interrupt Enable In) signals the MFP that no higher priority device is requesting the interrupt service (active LOW, internal pull-down). /MFPIEO signals that the MFP has no pending interrupts, and that /MFPIEI is active; i.e. no higher priority interrupt is pending. Thus, a multilevel structure can be obtained. Because many internal functions depend on the level 6 interrupts of the MFP, we recommend that external devices install themselves at a lower level, but do not require it.

To help in synchronization of external circuits (particularly when the Refresh Machine described above is running), a small number of clock signals are provided. They are:

- o CLK16                    main 16MHz clock
- o CLK8                    8MHz CPU clock
- o KHZ500                 500 KHz Baud Rate Clock

Some power and power control signals are provided to allow external devices to draw some power from the VCC supply of the STylus or STBook. To help distribute the power evenly, and to help maintain clean logic levels, there are 10 VCC signals, and 30 GROUND signals. 10 of the GROUND signals are located at the ends of the connector, opposite the VCC signals; the other 20 are distributed as every 5th pair of signals across the connector. This should aid in both maintaining a clean ground, and reducing EMI.

Power Control is possible to some degree using the signal /EXPANSION\_WAKE. This signal expects to be driven by an open-collector driver; when pulled to ground, this powers on the STylus/STBook. It is equivalent to pressing the Power button on either machine.

Finally, there is a pin which allows a peripheral plugged into the STBook or STylus to determine which it is connected to. Pin 94 is defined to be a no-connect on an STBook, and grounded on a STylus. The peripheral could, conceivably, determine the type of host without the host being powered; this is the responsibility of the peripheral, if it needs to know it.

The Expansion connector has the following pin assignments:

----- Expansion Port Pin Assignments -----

STBook	micro-D 120S		
1	VCC	GND	61
2	VCC	GND	62
3	VCC	GND	63
4	VCC	GND	64
5	VCC	GND	65
6	D0	D1	66
7	D2	D3	67
8	D4	D5	68
9	D6	D7	69
10	GND	GND	70
11	D8	D9	71
12	D10	D11	72
13	D12	D13	73
14	D14	D15	74
15	GND	GND	75
16	NC	A1	76
17	A2	A3	77
18	A4	A5	78
19	A6	A7	79
20	GND	GND	80
21	A8	A9	81
22	A10	A11	82
23	A12	A13	83
24	A14	A15	84
25	GND	GND	85
26	A16	A17	86
27	A18	A19	87
28	A20	A21	88
29	A22	A23	89
30	GND	GND	90
31	/HALT	/STylus	91
32	/MA	/CPUBG	92
33	/BR	/MCUBG	93
34	/BGACK	NC	94
35	GND	GND	95
36	FC0	FC1	96
37	FC2	/AS	97
38	R/W	/LDS	98
39	/UDS	/DTACK	99
40	GND	GND	100
41	/RESET	/VPA	101
42	/IPL0	/IPL1	102
43	/IPL2	/IACK	103
44	/EXPANSION_WAKE	/BERR	104
45	GND	GND	105
46	/MFPINT	/MFPIEI	106
47	/EINT3	/MFPIEO	107
48	/DMA	/DEV	108
49	/ROM3	/ROM4	109
50	GND	GND	110
51	NC	NC	111
52	NC	NC	112
53	CLK16	CLK8	113
54	KHZ500	E	114
55	GND	GND	115
56	VCC	GND	116
57	VCC	GND	117
58	VCC	GND	118
59	VCC	GND	119
60	VCC	GND	120