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SECTION ONE
INTRODUCTION

The Mega 2 and Mega 4 are Motorola MC68000 microprocessor based computers with similar architectures to the 520ST/ 1040ST line. They are styled as a main CPU unit with a detached keyboard. The Mega 2 has 2 megabytes of RAM, the Mega 4 contains 4 megabytes. Both the Mega 2 and Mega 4 have a built-in 1 Megabyte (720K formatted) 3.5 inch floppy disk drive, and an internal switching power supply with built-in cooling fan.

Since the only difference between the Mega 2 and Mega 4 is the size of its RAM, this manual will use ' Mega ' as a generic term which refers to both products.

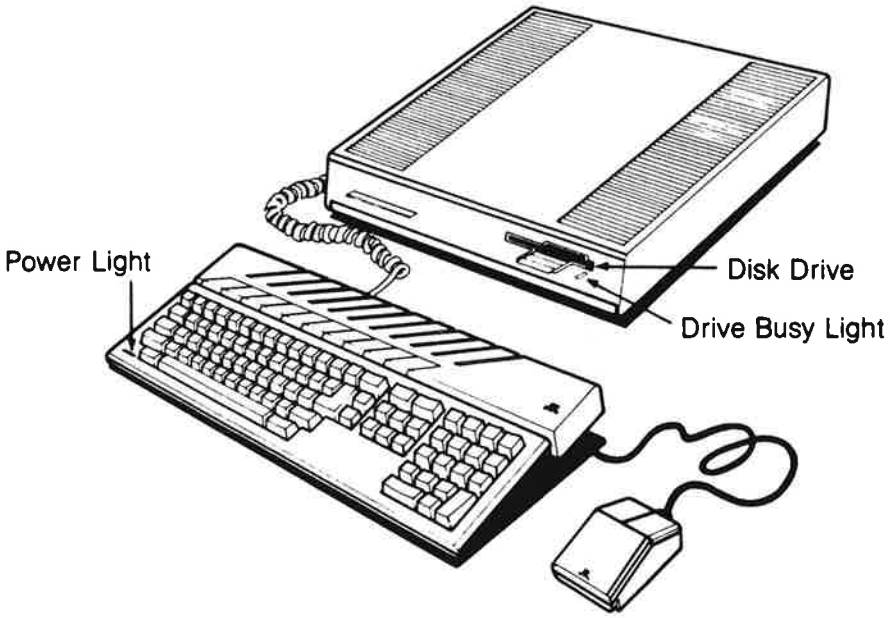


FIG. 1
MEGA COMPUTER SYSTEM

The main components of the Mega 2 and Mega 4 are:

CPU

- Main board assembly
- Disk drive
- Power supply & cooling fan
- RF Shield (upper and lower)
- CPU Plastic case (upper and lower)

KEYBOARD

- Keyboard assembly
- Interface board assembly
- Keyboard Plastics (upper and lower)

MOUSE

- Mouse board assembly
- Mouse Plastics (upper and lower)

CASE DESIGN

Figures 1 thru 4 shows the CPU portion of the MEGA, 5 and 6 shows the keyboard portion, and figure 7 shows the mouse.

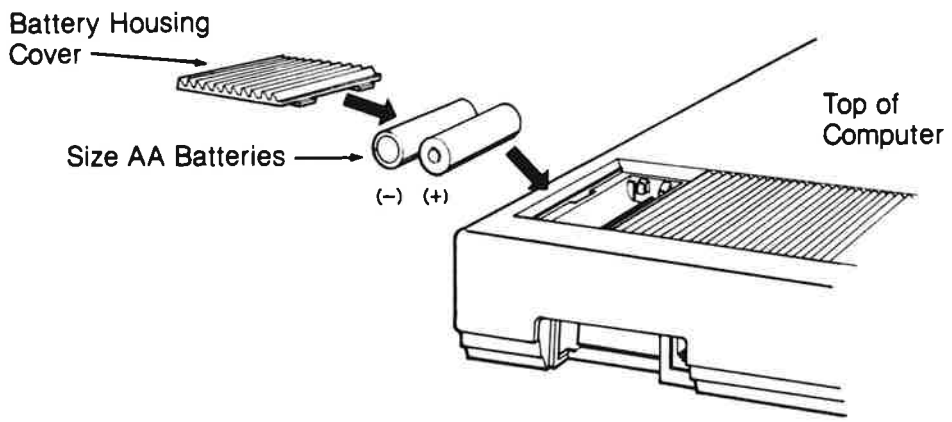


FIG. 2
BATTERY COMPARTMENT

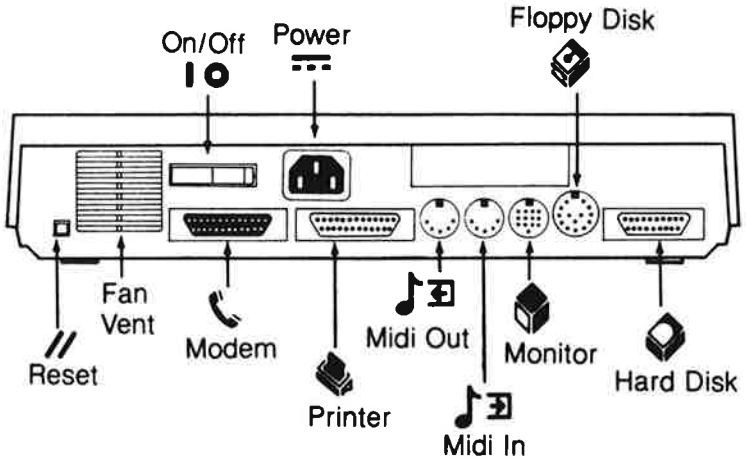


FIG. 3
BACK PANEL

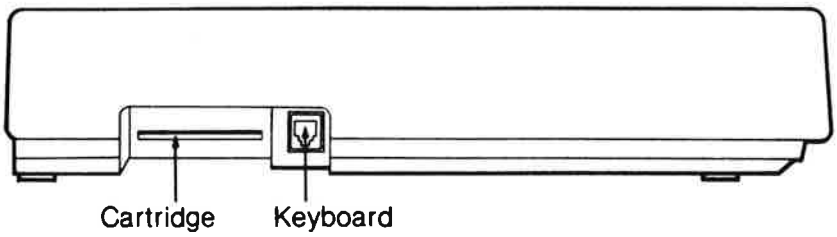


FIG. 4
LEFT SIDE PANEL

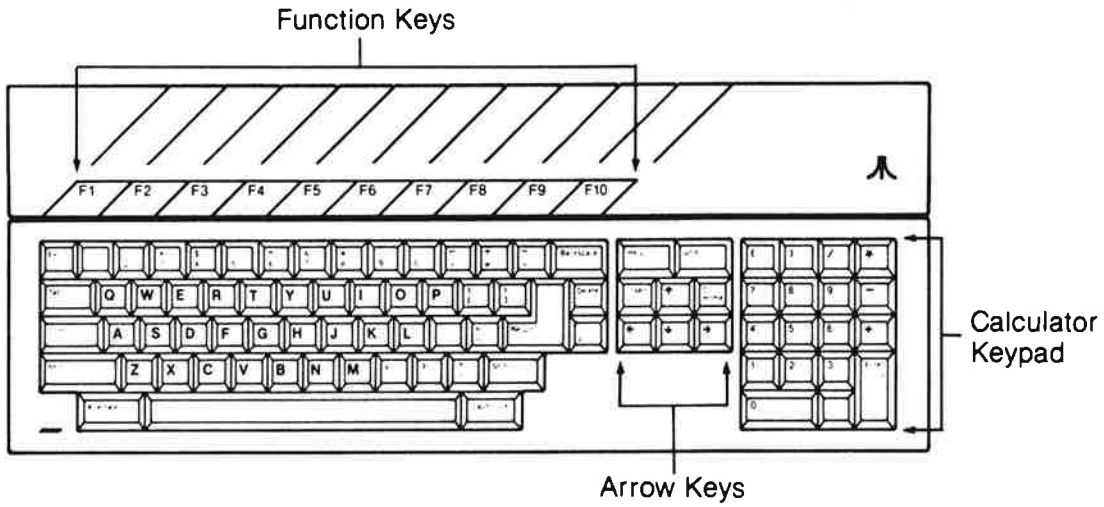


FIG. 5
TOP OF KEYBOARD

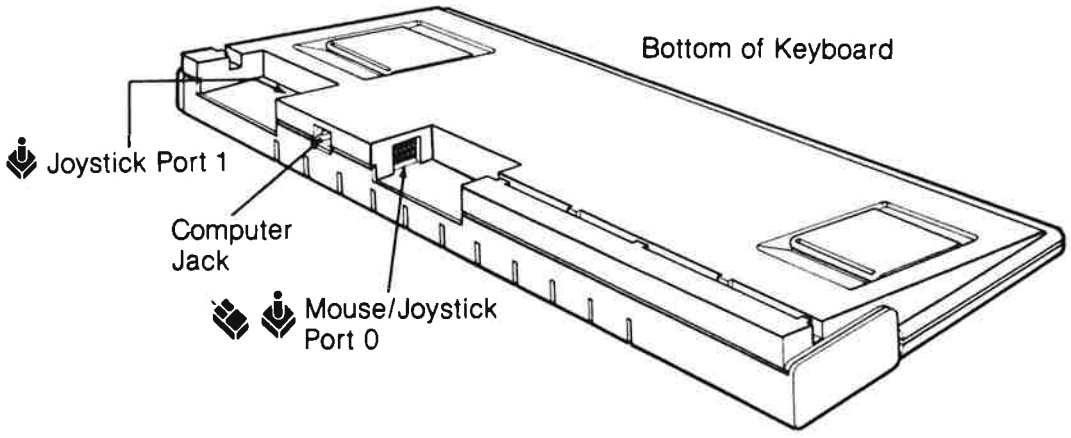


FIG. 5
BOTTOM OF KEYBOARD

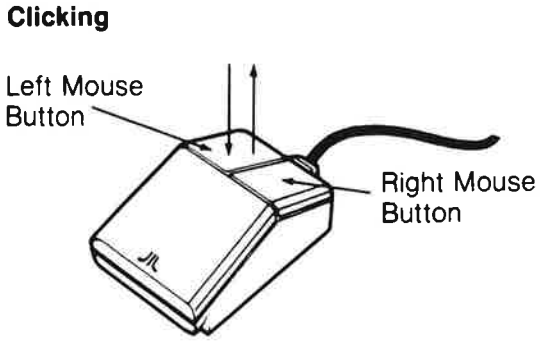


FIG. 7
MEGA MOUSE

Differences from 520ST/1040ST

- New version of TOS
- More memory requiring 74LS243 buffers on MAD lines
- Real time clock chip & support circuit
- Graphics Co-Processor (BITBLiT)
- Internal expansion connector & support circuit
- Cooling fan
- New case styling with detached keyboard

SECTION TWO
THEORY OF OPERATION

OVERVIEW

The Mega 2 and Mega 4 share a common architecture, using the same LSI chip set, and case styling. The only difference is the addition of one bank of 2 Mega-bytes of RAM, for a total of 4 Mega-bytes of RAM on the Mega 4. The hardware can be considered as consisting of a main system (central processing unit and support chips) and several Input/Output subsystems.

Main System

- MC68000 running at 8MHz
- 192 Kbyte Read Only Memory
- 2 or 4 Mega-byte Random Access Memory
- Direct Memory Access support
- System timing and Bus control
- Interrupt control

Audio/Video Subsystem

- Bit Mapped video display, using 32k bytes of RAM, relocatable anywhere in memory. There are three display modes available:
  a. 320 x 200 pixel, 16 color palette from 512 selections
  b. 640 x 200 pixel, 4 color palette from 512 selections
  c. 640 x 400 pixel, monochrome
- BITBLiT support
- Monitor interface analog: RGB, Monochrome
- Audio output: programmable sound chip with 3 voices

Input/Output Subsystems

- Intelligent Keyboard with 2 button mouse/joystick interface
- Parallel printer interface (Centronics)
- RS-232C serial interface
- DMA Port & connector for external drive
- Hard disk drive interface & Laser Printer
- Musical instrument network communication : Musical Instrument Digital Interface (MIDI).
- Real Time Clock with battery backup
- ROM Port

MAIN SYSTEM

The main system includes the microprocessing unit, main memory (ROM and RAM), system control, interrupt control, and general purpose DMA controller.

Microprocessing Unit

The Mega uses the Motorola MC68000 16 bit external/32 bit internal data bus, 24 bit address bus microprocessor, running at 8 MHz.

Glue

Glue (named because it holds the system together) is such an important component that it is involved in nearly every operation in the computer. The functions may be summarized as follows:

Clock dividers-- takes the 8 MHz clock and outputs 2 MHz and 500 KHz clocks.

Video timing-- Blank, DE (Display Enable), Vsync, and Hsync are used to generate signals for the video display. There is a Read/Write register in Glue which may be written to configure for 50 or 60 Hz operation (done by the Operating System).

Interrupt priority-- interrupts from the MFP and video timing are coded into four levels of priority on outputs IP11 and IPL2 to the 68000. These levels correspond to no interrupts, MFP interrupts, VSYNC interrupt, HSYNC interrupt.

Signal and Bus arbitration-- Glue decodes addresses to generate chip selects to the 6850s, MFP, DMA Controller, Programmable Sound Generator, Memory Controller, and ROMs. It receives signals from the MFP, DMA, Memory Controller, to synchronize data transfer. It arbitrates the bus during DMA transfers to prevent CPU and DMA devices from interfering with each other (see DMA below).

Illegal condition detection--Glue asserts Bus Error (BERR) if certain conditions are violated, such as writing to ROM, writing byte sized data to a word sized register, or writing to system memory when the processor is in user mode. Also occurs if a device does not respond within the required time limit. For example, the CPU tries to read from memory and the Memory Controller does not assert DTACK.

Main Memory

Main memory consists of 192 kbytes of ROM and one or two banks (2 Mega-byte each) of dynamic RAM. In addition, the cartridge slot allows access to 128 Kbytes of ROM. All memory is directly addressable. The components of the memory system are: ROM, RAM, RAM buffers, Memory Controller, and Glue. The Operating System resides mostly in ROM, with optional segments loaded from disk into RAM.

RAM is organized as 16 bit words and may be accessed 16 bits at a time or 8 bits at a time. Even numbered addresses refer to the high 8 bits of a word and odd addresses refer to the low 8 bits. RAM is made up of 1 Megabit X 1 chips; in the Mega 2 there are 16 chips, giving 2 Mbytes, while in the Mega 4 there is an additional bank of 16 chips, giving two times the memory, or 4 Mbytes.

RAM memory map:

000008-000800	System memory (priveliged access)
000800-1FFFFF	low bank
200000-3FFFFF	high bank (Mega 4 only)

Note: the first 8 bytes of ROM are mapped into addresses 0-7. These are reset vectors which the 68000 uses on start-up.

The Operating System is located in two 1Meg x 8 ROM chips in current versions (192k).

Memory Controller--takes addresses from the address bus and converts to Row Address Strobe (RAS) and Column Address Strobe (CAS). All RAM accesses are controlled by this Atari proprietary chip, which is programmable for up to 4 Megabytes of memory. The Operating System determines how much memory is present and programs the Memory Controller at power-up. The Memory Controller refreshes the dynamic RAMs, loads the Video Shifter with display data, and gives or receives data during direct memory access (DMA).

Glue--decodes addresses for RAM and ROM and asserts output signals to enable these devices (also decodes addresses for most hardware registers to provide chip selects, as well as many other functions. See Glue description above.).

Direct Memory Access

Direct memory access is provided to support both low speed (250 to 500 Kilobits/sec) and high speed (up to 8 Megabits/sec) 8bit device controllers. The floppy disks transfer data via low speed DMA and the hard disk (or other devices on the hard disk port) transfer at high speed. For DMA to take place, the Memory Controller is given the address of where to take data from or put data in RAM, the DMA Controller is set up (which channel, high speed or low speed, and how many bytes) and the peripheral is given a command to send or receive data. The entire block of data (the size must be given to the DMA Controller and the peripheral before the operation starts) is then transferred to or from memory without intervention by the CPU.

For example, in a transfer of a sector from the floppy to memory, the floppy controller will signal the DMA Controller that a byte is ready by asserting FDRQ, the DMA chip will read the byte and signal Glue, Glue will signal the Memory Controller, and the Memory Controller will read the byte from the DMA Controller and place it in the address which was set up previously. The DMA Controller will then wait for the next byte from the floppy controller, and the process will repeat until the specified number of bytes has been transferred. Transfers from memory to floppy are similar. The floppy initiates every transfer by requesting data on FDRQ.

At high speed (hard disk port), there is a difference: as a byte is ready to transfer to or from the DMA chip, the DMA Controller will assert ACK to let the peripheral know the byte is available or has been read. The DMA Controller can store up to 32 bytes in internal memory. This is necessary if the 68000 is using the bus, and the DMA must wait to transfer to memory. Data may be input from the port without being lost or slowing down the transfer speed.

MFP Interrupt Control

The 68901 MFP handles up to 16 interrupts. Currently all but one are used. Each interrupt can be masked off or disabled by programming the MFP. The 8 inputs are also directly readable by the CPU. When the MFP receives an interrupt input, or generates an interrupt internally, if the interrupt is enabled, MFPINT will be driven low. When the CPU is ready to respond, it signals interrupt acknowledge (FC0-2 high and VMA low) and Glue will assert IACK (interrupt acknowledge). The MFP will assert DTACK and put a vector number on the data bus, which the CPU will read and use to calculate the address of the interrupt routine.

The interrupts controlled by the MFP are: monochrome monitor detect (MONOMON), RS232 (including CTS, DCD, RI), disk (FDINT and HDINT), parallel port BUSY, display enable (DE, equals start of display line), 6850 IRQs for keyboard and MIDI data, and MFP timers.

Not all I/O operations use interrupts. The CPU can also poll the MFP while waiting for an operation to complete. The MFP has four timers, used by the Operating System for event timing and used by the RS232 port for transmit and receive clocks.

AUDIO/VIDEO SUBSYSTEM

The video subsystem consists of the video display memory, the Memory Controller, Glue, a graphics control chip (Video Shifter), a graphics processing unit (BITBLiT), and a discrete section to drive the video output. The audio subsystem consists of a Programmable Sound Generator chip with a transistor output amplifier.

Video Shifter

There are 16 color palette registers in the shifter. All 16 are may be used in low resolution, 4 may be used in high resolution, and only one is used in high resolution (actually, only bit 0 of register 0 is used for inverse/normal video). Each palette is programmed for 8 levels of intensity of red, blue, and green, so there are 8 x 8 x 8 = 512 colors possible. For a given pixel, the color which is displayed is taken from the palette referred to by getting information from each logical plane (see description of video display memory below). The shifter will output the red, green, and blue levels specified by that palette; note there are three outputs for each color. Each output is either on or off. Thus, the number of possible output levels is 2 to the 3rd power = 8. The three outputs are summed through a resistor network to proportion the voltage level to give 8 equal steps. In monochrome mode, the color palettes are bypassed and there is a separate output.

Video Display Memory

Display memory is part of main memory with the physical screen origin located at the top left corner of the screen. Display memory is configured as 1, 2, or 4 (high, medium, or low resolution) logical planes interwoven by 16 bit words into contiguous memory to form one 32 Kilobyte physical plane starting at a 256 byte half page boundary. The starting address of display memory is placed in the Memory Controller's Video Base Address register by the Operating System or application. The Memory Controller will load display information into the Video Shifter 16 bits at a time, and the Video Shifter will decode this information to generate a serial display stream. In monochrome mode, each bit represents 1 pixel on or off. In color, bits are combined from each plane to generate the correct level of red, green, and blue.

For example, in low resolution (4 planes) 4 words are loaded into the Video Shifter for each word (16 pixels displayed on the screen. The Video Shifter combines bit 0 from each word to form a four bit number (0-15), and takes the color from the palette referenced by that number (e.g. 0101=5, use color from palette register 5) and outputs those levels, then takes bit 1 from each plane and outputs the color from the palette referenced by those four bits, etc.

Glue

Glue provides timing control to the Memory Controller, video output, and monitor/RF output. VSYNC input to the Memory Controller causes the starting address of the display memory to be reloaded into the address counter during vertical blanking. DISPLAY ENABLE (DE) tells the Memory Controller and Video Shifter that a display line is being scanned and data should be loaded into the Video Shifter. BLANK shuts off the video output from the Video Shifter during periods when the scan is not in a displayable part of the screen. VSYNC and HSYNC both go to the monitor output and RF modulator. These signals synchronize the monitor or T.V. vertical and horizontal sweep to the display signal.

Memory Controller

In addition to the inputs from Glue mentioned above, there are two output control signals associated with video. DCYC strobes data from display memory into the Video Shifter. CMPCS (color map select) is active only when changing the color attributes in the color palettes.

Sound Synthesizer

The YM2149 Programmable Sound Generator (PSG) produces music synthesis, sound effects, and audio feedback (e.g. alarms and key clicks). The clock input is 2 MHz; the frequency response range is 30 Hz to 125 KHz. There are three sound channels output from the chip, which are mixed and sent to the monitor speaker.

The PSG is also used in the system for various I/O functions relating to printer port, disk drive, and RS232.

Atari Blitter

This is a DMA device that moves block of memory data from a source location to a destination location through a given logic operation. Single or multiple word increments and decrements are provided for transfer to destination. There are 16 possible logic operation rules associated with the merging of source and destination data. In addition, with the 16 word patterns ram and three 16 bit end-mask registers, the blit can also be used to perform operations such as area seed filling, pattern filling, brush line drawing, text and graphic transformations, etc.

For more information, please refer to the user manual which is included in the Developer Kit.

Real Time Clock with Battery Backup

This device has counters for Time and Calendar built-in. Clock data are expressed with BCD code. The lower four address and data lines are used to program the device and access the clock through signal lines RTCCS, RTCRD, RTCWR which generated from a decoder. A RESET line is also provided to reset the chip when the system is reset. The main clock supplied to the device is a 32.768 Khz oscillator which will be adjusted by a trimmer condenser so that it will output through the CLKOUT line a standard clock signal of 16.384 Khz. In addition, a 3V battery backup can be used to keep the clock running during power down.

For more detail, please refer to the application manual from the manufacturer (RICOH part number RP5C15)

Video Interface

The two types of interface are provided in the Megas are analog RGB and monochrome. The presence of a monochrome monitor is detected by the MONOMON input (when a monochrome monitor is connected, it will be low). The possible displays are:

Monochrome: single emitter follower amplifier driving the output of the Video Shifter.

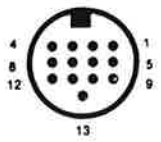
RGB: resistor network sums outputs for each color. The three colors each have an emitter follower amplifier to drive output.

Monitor Inputs:

Hsync--TTL level, negative, 3.3 k ohm.
Vsync--TTL level, negative, 3.3 k ohm.
Monochrome--digital 1.0V P-P, 75 ohm.
R,G,B--analog 0-1.0V P-P, 75 ohm.
Audio--1V. P-P, 1k ohm.

Monitor

1 — Audio Out
2 — Composite Sync
3 — General Purpose Output
4 — Monochrome Detect
5 — Audio In
6 — Green
7 — Red
8 — Plus 12-Volt Pullup
9 — Horizontal Sync



10 — Blue
11 — Monochrome
12 — Vertical Sync
13 — Ground

FIG. 8
MONITOR PORT

Musical Instrument Communication

The Musical Instrument Digital Interface (MIDI) allows the integration of the Mega with music sysnthesizers, sequencers, drum boxes and other devices possessing MIDI interfaces. High speed (31.25 Kilobaud) asynchronous current loop serial communication of keyboard and program information is provided by two ports, MIDI OUT and MIDI IN (MIDI OUT also supports the optional MIDI THRU port). MIDI specifies that data consist of 8 data bits preceded by one start bit and followed by one stop bit.

Communication takes place via a 6850 ACIA. The CPU reads and writes to the 6850 in response to interrupts which are passed from the 6850 to the MFP interrupt controller. The system is interfaced to the outside via two inverters on the transmit side and an LED/photo-transistor chip on the input side. The input signal is routed around through two inverters to the output connector where it is called MIDI THRU in order to allow chaining of multiple devices on the MIDI bus.

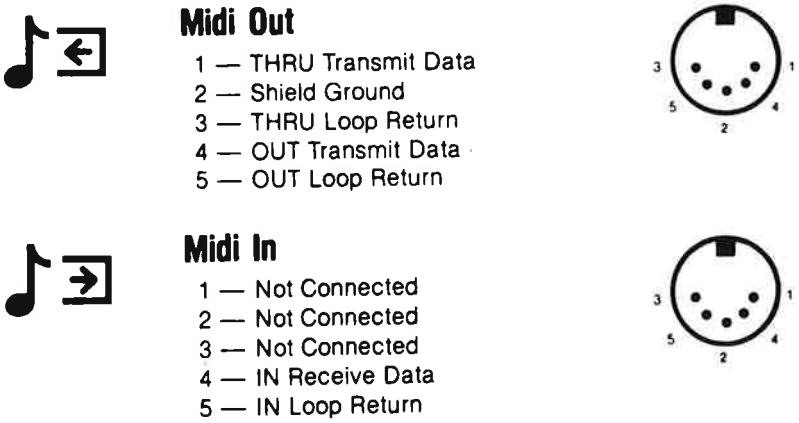


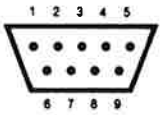
FIG. 9
MIDI PORTS

Intelligent Keyboard

The keyboard transmits make/break key scan codes, ASCII codes, mouse data, joystick data, in response to external events, and time-of-day data (year, month, day, hour, minute, second) in response to requests by the CPU. Communication is controlled on the main board by a 6850 device and on the keyboard assembly by the 1MHz 8 bit HD6301 Microcomputer Unit. The HD6301 has internal RAM and ROM. Included in ROM are self-test diagnostics which are performed at power-up and whenever the RESET command is sent over the serial communication line by the CPU. The MC6850 is read and written to by the CPU in response to interrupts which are passed to the CPU by the MFP interrupt controller.

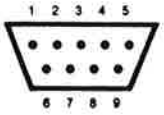
The 2 Button Mouse is an opto-mechanical device with the following characteristics: a resolution of 100 counts/inch, a maximum velocity of 10 inches/second and a maximum pulse phase error of 50 percent. The joystick/mouse port has inputs for up, down, left, right, right button, left button. The right button equals the joystick trigger, and the left button is wired to the second joystick port trigger. The joystick has four directions (up, down, etc.) and one trigger.

Mouse / Joystick



1 — Up/XB
2 — Down/XA
3 — Left/YA
4 — Right/YB
5 — Not Connected
6 — Fire/Left Button
7 — + 5VDC
8 — Ground
9 — Joy1 Fire/Right Button

Joystick



1 — Up
2 — Down
3 — Left
4 — Right
5 — Reserved
6 — Fire Button
7 — + 5VDC
8 — Ground
9 — Not Connected

FIG. 10
MOUSE/JOY PORT

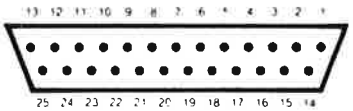
Parallel Interface

The parallel port is primarily intended as a Centronics type printer interface, but can also be used as a general purpose I/O port. Centronics STROBE and BUSY are supported. BUSY is read by the MFP chip. Data and strobe signals are output by the YM2149 PSG chip. Not all Centronics printers are compatible with this port. The current loading on the data lines should not exceed 2.3 mA. (This corresponds to a 2.2k ohm resistor pull-up on the printer side.)

The port can be programmed to be input or output. The PSG chip is read directly by the CPU, with Glue doing address decode to provide chip select.

Printer

1 — STROBE Output
2 — Data 0
3 — Data 1
4 — Data 2
5 — Data 3
6 — Data 4
7 — Data 5
8 — Data 6
9 — Data 7



10 — Not Connected
11 — BUSY Input
12-17 — Not Connected
18-25 — Ground

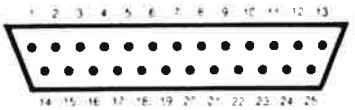
FIG. 11
PRINTER PORT

RS232C Interface

The RS232C interface provides asynchronous serial communication with five handshake control signals: Request to Send and Data Terminal Ready are output by the PSG chip; Clear to Send, Data Carrier Detect, and Ring Detect are input to the MFP chip. The MFP contains a USART (Universal Synchronous/Asynchronous Receiver/Transmitter) which handles data transmission and reception. The 2.4576 MHz clock to the MFP is divided by the timer D (pin 16) output of the MFP to provide the basic clock for receiver and transmitter. Data rate of 50 to 19200 bits per second are supported. 1488 line drivers and 1489 line receivers with +/- 12v. supply meet the EIA RS232C standard for electrical interface.

Modem

1 — Protective Ground
2 — Transmitted Data
3 — Received Data
4 — Request to Send
5 — Clear to Send
6 — Not Connected
7 — Signal Ground
8 — Data Carrier Repeat
9-19 — Not Connected



20 — Data Terminal Ready
21 — Not Connected
22 — Ring Indicator
23-25 — Not Connected

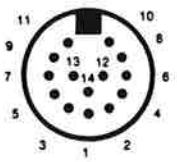
FIG. 12
RS232 PORT

Disk Drive Interface

The Mega computers have a built-in floppy disk controller (a Western Digital 1772) and logic for selecting up to two single or double sided drives. The Mega has one built-in floppy disk drive and provision for one external disk drive. The Western Digital WD1772 Controller services both drives. Drive and side selection is done by outputs on the YM2149 PSG chip. The CPU reads and writes to the 1772 through the DMA Controller. The 1772 interrupts the CPU on the INTR line, via the MFP interrupt controller. The 1772 accepts high level commands, such as seek, format track, write sector, read sector, etc. and passes data to the DMA Controller (see DMA controller under Main System, above, for details on DMA transfer). The 1772 interrupts the CPU when the operation is complete. The CPU is freed from much of the overhead of disk I/O.

Floppy Disk

1 — Read Data
2 — Side 0 Select
3 — Logic Ground
4 — Index Pulse
5 — Drive 0 Select
6 — Drive 1 Select
7 — Logic Ground
8 — Motor On
9 — Direction In
10 — Step



11 — Write Data
12 — Write Gate
13 — Track 00
14 — Write Protect

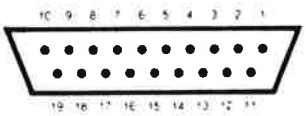
FIG. 13
EXTERNAL FLOPPY PORT

DMA Port; Hard Disk Interface

The hard disk drive interface is provided through the DMA controller; the hard disk controller is off-board and is board and is sent commands via an SCSI-like (Small Computer System Interface) command parameter block. Data is transferred via DMA. Writing to the external controller causes HDCS (Hard Disk Chip Select) to go low and CA1 to go high. DMA transfers are controlled by the external device. When data is available, or the device is ready to accept data, HDRQ will be driven high by the external controller. The DMA chip must respond within 250 nanoseconds with ACK (low) to acknowledge that data is on the bus or has been read from the bus. The Memory Controller feeds data to or accepts data from the DMA Controller. Transfers can take place at up to 1 Mbyte/second.

Hard Disk

1 — Data 0
2 — Data 1
3 — Data 2
4 — Data 3
5 — Data 4
6 — Data 5
7 — Data 6
8 — Data 7
9 — Chip Select
10 — Interrupt Request
11 — Ground
12 — Reset



13 — Ground
14 — Acknowledge
15 — Ground
16 — A1
17 — Ground
18 — Read/Write
19 — Data Request

FIG. 14
EXTERNAL HARD DISK PORT

SYSTEM STARTUP

After a RESET (power-up or reset button) the 68000 will start executing at the address pointed to by locations 4-7, which is ROM (Glue maps 8 bytes of ROM at FC0000-7 into the addresses 0-7). Location 000004 points to the start of the operating system code in ROM (FC0000-FEFFFF). The following sequence is then executed:

1. Perform a reset instruction (outputs a reset pulse).
2. Read the longword at cartridge address FA0000. If the data read is a "magic number", execute from the cartridge (diagnostic cartridge takes over here). If not, continue.
3. Check for a warm start (see if RAM locations were previously written), initialize the memory controller, and continue running the application which was running before the reset if it was a warm start.
4. Initialize the PSG chip, deselect disk drives.
5. Initialize color palettes and set screen address.
6. If not a warm start, zero memory.
7. Set up operating system variables in RAM.
8. Set up exception vectors.
9. Initialize MFP.
10. Set screen resolution.
11. Attempt to boot floppy; attempt to boot hard disk; run program if succeeded.

SYSTEM ERRORS

The 68000 has a feature called exception processing, which takes place when an interrupt or bus error is indicated by external logic, or when the CPU detects an error internally, or when certain types of instructions are executed. An exception will cause the CPU to fetch a vector (address to a routine) from RAM and start processing at the routine pointed to by the vector. Exception vectors are initialized by the operating system. Those exceptions which do not have legitimate occurrences (interrupts being legitimate) have vectors pointing to a general purpose routine which will display some number of bombs showing on the screen (mushroom clouds in older versions of disk loaded operating system). The number of bombs equals the number of the exception which occurred.

System errors may or may not be recoverable. Errors in loading files from disk will cause the system to crash, necessitating a reset. Verify the diskette and disk drive before attempting to repair the computer.

NUMBER OF BOMBS AND MEANINGS
(No. 26,28,30, and 64-79 will not bomb, as they are legitimate.)

2 Bus Error. Glue asserted bus error or CPU detected an error.
3 Address Error. Processor attempted to access word or long word sized data on an odd address.
4 Illegal Instruction. Processor fetched an instruction from ROM or RAM which was not a legal instruction.
5 Zero Divide. Processor was asked to perform a division by zero.
6 Chk Instruction. This is a legal instruction, if software uses this, it must install a handler.
7 Trapv Instruction. See Chk instruction.
8 Privilege Violation. CPU was in user mode, tried to access a location in supervisor address space.
9 Trace. If trace bit is set in the status register, the CPU will execute this exception after every instruction. Used to debug software.
10 Line 1010 Emulator. CPU read pattern 1010 as an instruction. Provided to allow user to emulate his own instructions.
11 Line 1111 Emulator. See Line 1010 Emulator.
12-23 Unassigned, should be no occurrence.
24 Spurious Interrupt. Bus error during interrupt processing.
25-31 Autovector Interrupt. Even numbered vectors are used, others should have no occurrence.
32-63 TRAP Instruction. The CPU read instruction which forced exception processing.
64-79 MFP interrupts.
80-255 User interrupts.

Note: If you have an error message such as "TOS ERROR 35", then the possible errors are:

1- The file in progress is bad.
2- The total number of folders in the system has exceeded the 40-folder limit. However, there is a program which can be used to extend this limitation on folders.
3- No handles left or too many open files.